

REMARKS

Reconsideration and further examination of the application as amended are respectfully requested. All objections and rejections are traversed.

The Office Action objected to an informality that was found in the Specification at page 3, line 11. Applicant has amended this paragraph to correct the informality. Applicant has also amended the Specification at pp. 2, 4 and 6 to correct other minor informalities that have been discovered in the text.

The Office Action also objected to an informality found in claim 2. Applicant has amended claim 2 to correct the informality. In addition to claim 2, Applicant also amended claims 1, 4 and 7 to correct other minor, typographical errors. No new matter is being introduced. In light of these amendments, Applicant requests that the objections to the Specification and claims be withdrawn.

In the Office Action, claims 1-3 and 5-7 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,114,917 to Nakajima et al. ("Nakajima"). Claims 4 and 8 were rejected under 35 U.S.C. §103 as obvious based on Nakajima in view of U.S. Patent No. 5,822,317 to Shibata ("Shibata"). Applicant respectfully traverses the rejection.

Claim 1, as amended, recites as follows:

An error detection system for a clock signal comprising:
a first counter that receives and counts the clock signal,
a phase-locked loop circuit that receives the clock signal and outputs a second clock signal,
a second counter that receives and counts the second clock signal,

a comparator that receives and compares the outputs of the first and the second counters, and

an error output from the comparator that is true when the counts of the first and second counters are unequal.

As shown, claim 1 recites an error detection system that comprises, among other things, two counters, a Phase Lock Loop (PLL) circuit and a comparator. The Office Action cites to element 1 (Fig. 1) of Nakajima as disclosing the claimed first counter, elements 4 and 5 (Fig. 1) as disclosing the claimed PLL circuit, element 6 (Fig. 1) as disclosing the second counter, and element 2 (Fig. 1) as disclosing the comparator. Applicant respectfully contends that Nakajima fails to disclose the invention as recited.

First, Fig. 1 of Nakajima does not disclose an error detection system. Instead, it shows Nakajima's analog PLL circuit. This is confirmed by Nakajima in several places. See Col. 4, lines 11-12 ("FIG. 1 is a circuit diagram of a first embodiment of **an analog PLL circuit** according to the present invention"), and Col. 4, lines 34-35 ("FIG. 1 is a circuit diagram of a first embodiment of **an analog PLL circuit** according to the present invention"). In contrast, claim 1 recites an error detection system, just one element of which is a phase-locked loop (PLL) circuit.

Second, the individual elements of Nakajima's analog PLL circuit do not correspond to the claimed error detection circuit. For example, element 1 of Nakajima's analog PLL circuit is a divider, and not a counter as is recited in claim 1. See Col. 4, line 40 ("the divider 1), line 51 ("The divider 1"). Similarly, elements 4 and 5 of Nakajima's analog PLL circuit correspond to a low pass filter and a voltage controlling oscillator, respectively. See Col. 4, lines 41-42 ("the low pass filter 4, the voltage controlling oscil-

lator”). Indeed, these two elements Nakajima could not possibly correspond to a PLL circuit, because it is the complete set of elements shown in Fig. 1 of Nakajima that correspond to its analog PLL circuit. Thus, by definition, none of Nakajima’s individual components could themselves correspond to a PLL.

Furthermore, element 6 of Nakajima’s analog PLL circuit is another divider, not a second counter as recited in claim 1. See Col. 4, line 42 (“divider 6”), line 52 (“divider 6”). Nakajima, moreover, makes clear that its dividers (elements 1 and 6), far from providing any counts, instead output signals that are fractions of the frequency of an input signal. See Col. 4, lines 51-52 (“The divider 1 outputs a signal with the frequency of a Mth part of the standard input signal, and the divider 6 outputs a signal with the frequency of a Nth part of the standard input signal”).

As shown, Nakajima fails to disclose any counters whatsoever. Nakajima also fails to disclose a PLL that receives a first clock signal and outputs a second clock signal. Instead, Nakajima’s low pass filter (element 4) simply “eliminates unnecessary high-frequency” noise, and its voltage controlling oscillator (element 5) provides an “oscillating function”. See Col. 4, line 62-63 and Col. 5, lines 5-6. Because Nakajima fails to disclose two dividers or a PLL circuit that receives a first clock signal and outputs a second clock signal, the rejection of claim 1 should be withdrawn. The rejection of claims 2-3, which depend from claim 1, should also be withdrawn. Similarly, the rejection under §103 of claim 4 based in part on Nakajima should also be withdrawn as claim 4 depends from claim 1, which is distinguishable over Nakajima.

Claim 5, which is directed to a method for detecting clock signal errors, recites in relevant part:

“a first counting of the first clock signals”,

“a second counting of the second clock signals”,

“detecting a difference between the first and the second countings”, and

“signaling an error therewith”.

As described above, Nakajima fails to disclose the counting of any clock signals.

Nakajima also fails to disclose detecting a difference between first and second countings, and signaling an error therewith. The Office Action cites to element 3 (Fig. 1) of Nakajima as signaling an error. Applicant respectfully disagrees. Element 3 of Nakajima corresponds to a charge pump that, instead of issuing any error indication, simply performs charge and discharge functions. See Col. 4, lines 59-60 (“The charge pump 3 performs charge and discharge in accordance with the UP signal and the DOWN signal in order to adjust the input level of the low pass filter”). Because Nakajima fails to disclose counting first and second clock signals, detecting a difference between those counts and signaling an error, the rejection of claim 5 should be withdrawn. The rejection of claims 6-7 should also be withdrawn as they depend from claim 5.

Similarly, the rejection under §103 of claim 8, which depends from claim 5, based in part on Nakajima should be withdrawn as claim 5 is distinguishable over Nakajima.

New claims

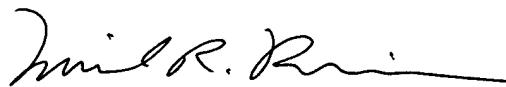
Applicant has added new claims 9-14. No new matter is being introduced. In particular, support for the new claims may be found in the Specification as originally

filed at pp. 5-7 and Fig. 4, among other places. New claims 9-14 contain numerous recitations that are neither disclosed nor taught by the art of record.

Applicant submits that the application, as amended, is in condition for allowance and early favorable action is requested.

It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's deposit account no. 08-2025.

Respectfully submitted,



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